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		REPRENTATIVE DIVISION ENGINEERING DEPARTMENT 2 DUTY PANEL DEVELOPMENT CENTER NARA LIQUID CRYSTAL DISPLAY GROUP
	SPECIFICATION	

DEVICE SPECIFICATION for

Passive Matrix Color LCD Module

(800x600 dots)

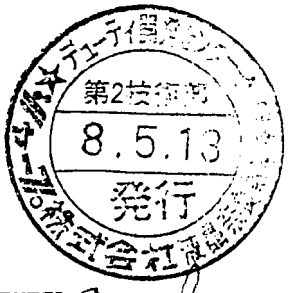
Model No.

LM80C36

☐CUSTOMER'S APPROVAL

DATE

BY



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SHARP

SPEC No.	MODEL No.
LC96507	LM80C36

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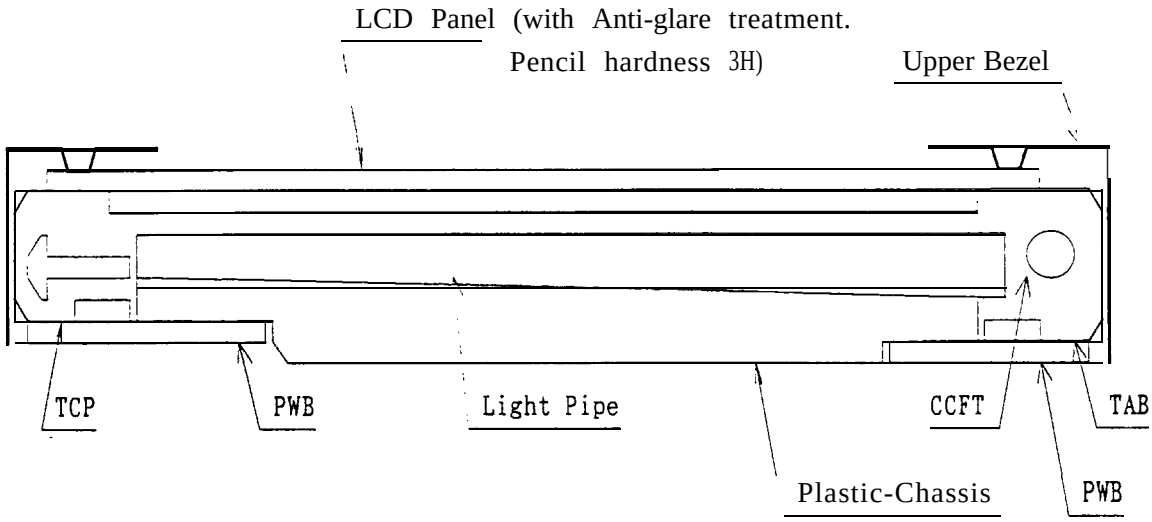
DATE	REF. PAGE PARAGRAPH DRAWING No.	REVISED No.	SUMMARY	CHECK & APPROVAL

1. Application

   This data sheet is to introduce the specification of LM80C36, Passive Matrix type Color LCD Module.

2. Construction and Outline

   Construction: 800x600 dots color display module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.
   Signal ground(V_{ss}) is connected with the metal bezel.
   DC/DC converter is built in.



Outline : See Fig. 10
Connection : See Fig. 10 and Table 6

3. Mechanica Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	275.0 (W) X199.0 (H) X8.5MAX(D)	mm
Effective viewing Area	250.0 (W) X187. O(H)	mm
Display format	800(W) X600(H)	—
Dot size	0.0775 xRGB(W) X0.2800(H)	mm
Dot spacing	0.025	mm
*1 Base color	Normally black *2	—
Weight	530 ± 15	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display

Display data "H" : ON → transmission

Display data "L" : OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum rat ngs

Table 2

Parameter	Symbo 1	MIN.	MAX.	Unit	Remark
SupplY voltage (Logic)	V_{DD}-V_{ss}	0	6.0	V	Ta=25 ℃
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V	Ta=25 "C
Vcon voltage	Vcon	0	V_{DD}	v	Ta=25 "C

4-2 Environments Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 “C	+60 “C	0 ℃	+40 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 ℃ . . . ..80 % RH Max

Ta>40 ‘C.. . . .Absolute humidity shall be less than Ta=40 “C/80 % RH.

Note 2)

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	–	9.8 m/s’
Vibration width	0.075 mm	–
Interval	10 Hz～500 Hz-10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction of ±X/±Y/±Z

Note 4) Care should be taken so that the LCD module may not be subjected to the temperature out of this specification.

5. Electrical Specifications

5-1 Electrical characteristics

(1/tFRM=120Hz)

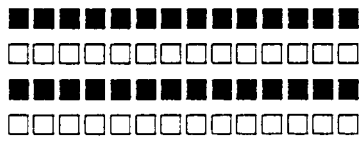
Table 5 Ta=25 "C V_{DD}=3.3 V± 10 %

Parameter	Symbo 1	Conditions	Min.	Typ.	Max .	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Ta=0～40 "C Note 1)	3.0	3.3	3.6	v
Contrast adjust voltage (Note 2)	Vcon-Vss	Ta= O "C	1.0			
		Ta= 25 "C		1.95		
		Ta= 40 ℃			2.5	v
Input signal voltage	V_{IN}	"H" level	0.8 V_{DD}	'	V_{DD}	v
		"L'" level	0	—	0.2V_{DD}	v
Supply current	I_{DD}1(TYP)	Ta=25 "C Note 1,2)	"	270	410	MA
	I_{DD}2(MAX)	Ta=25 ℃ Note 1,3)	—	360	540	MA
Rush current (Logic)	I rush	Ta=25 "C,	2 A(pk)×50 ms			
Ripple current (Logic)	Irip	Ta=25 "C,	1 A(pk)×100 μs			
Power consumption	Pd1(TYP)	Note 1,2)	—	890	1 335	mW
	Pd2(MAX)	Note 1,3)	—	1 190	1 780	mW

Note 1 Under the following conditions. ;
①Immediately after the rise of V_{DD}. : 2 A(pk)×50 ms
②Under the situation that DISP signal is on and kept steady.: 1 A(pk)×100 *us*

Note 2 Frame frequency = 120 Hz, Vcon-Vss = 1.95 V
Display pattern = all digits ON (DUO-7, DLO-7 = ' H')

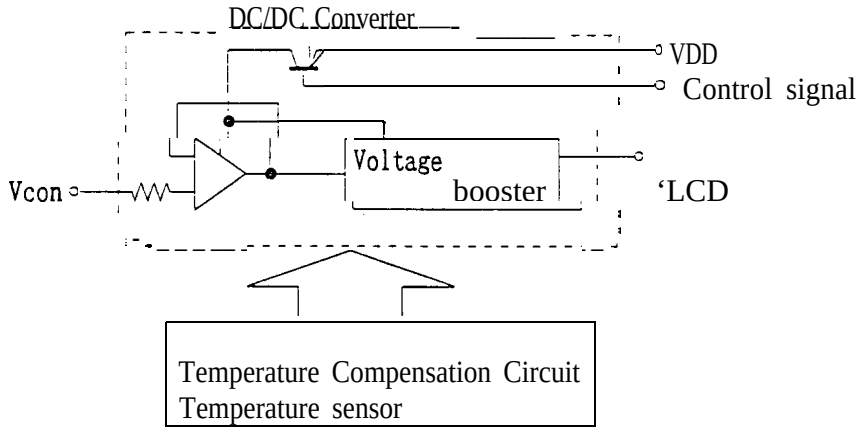
Note 3) Frame frequency = 120 Hz, Vcon-Vss = 1.95 V
Display pattern ❑ black/white stripe patten



Note 4) Contrast adjustment voltage "Vcon-Vss" is transformed into the LCD driving v oltage "V_{LCD}" by following circuit built in the LCD module.
LCD driving voltage "V_{LCD}" is adjusted automatically according to the change of ambient temperature range by the temperature compensation circuit.
Temperature compensation circuit built in LCD module have been set obtain the optimum contrast under following driving condition ;
Take care that voltage for optimum contrast is changed under the different condition.

Frame frequency : 120 Hz, Duty ratio : 1/300 (an odd number frame), Ta= 25 "C
1/328 (an even number frame)

※The above is the condition of the module setting,not the electrical characteristics.



3-2 Interface signals

○LCD

Table 6

Pin No	Symbo 1	Description	Level
1	V s s	Ground potential	–
2	XCK	Data inoput clock signal	" H " →" L "
3	V s s	Ground potential	–
4	V s s	Ground potential	–
5	L P	Input data latch signal	" H " →" L "
6	YD	Scan start-up signal	" H"
7	V s s	Ground potential	–
8	V s s	Ground potential	–
9	VDD	Power supply for logic and LCD	–
10	D I S P	Display control signal	H (ON) , L(O F F)
11	V s s	Ground potential	·
12	V s s	Ground potential	–
13	V s s	Ground potential 1	-
14	D L 7	Display data signal (Lower)	H (ON) , L (OFF)
15	D L 6	Display data signal (Lower)	H (ON) , L (OFF)
16	DL5	Display data signal (Lower)	H (ON) , L (OFF)
17	D L 4	Display data signal (Lower)	H (O N) , L (O F F)
18	DL3	Display data signal (Lower)	H (O N) , L (O F F)
19	DL2	Display data signal (Lower)	H (O N) , L (O F F)
20	D L 1	Display data signal (Lower)	H (O N) , L (O F F)
21	DLO	Display data signal (Lower)	H (O N) , L (O F F)
22	V s s	Ground potential	–
23	V s s	Ground potential	-
24	V s s	Ground potential	–
25	DUO	Display data signal (Upper)	H (O N) , L (O F F)
26	D U 1	Display data signal (Upper)	H (O N) , L (O F F)
27	DU2	Display data signal (Upper)	H (O N) , L (O F F)
28	DU3	Display data signal (Upper)	H (O N) , L (O F F)
29	DU4	Display data signal (Upper)	H (O N) , L (OFF)
30	D U 5	Display data signal (Upper)	H (ON) , L (OFF)
31	DU6	Display data signal (Upper)	H (O N) , L (OFF)
32	DU7	Display data signal (Upper)	H (ON) , L (OFF)
33	V s s	Ground potential	–
34	V s s	Ground potential	–
35	V s s	Ground potential	–
36	VDD	Power supply for logic and LCD	–
37	VDD	Power supply for logic and LCD	–
38	V c o n	Contrast adjust voltage	–
39	NC		–
40	V s s	Ground potential	–
41	V s s	Ground potential	–

3-2 Interface signals

Oc CFT

Pin No	Symbol	Description	Level
1	HV	High voltage line (from Inverter)	–
2	NC		–
3	GND	Ground line (from Inverter)	

OLCD

Used connector: IL-310-41P-VF(JAE)
Correspondable connector:IL-310-41S-VF(JAE)

OCCFT

Used connector:BHR-03VS-1 (JST)
Correspondable connector: SM02(8.O)B-BHS(JST)

Except above connector shall be out of guaranty.

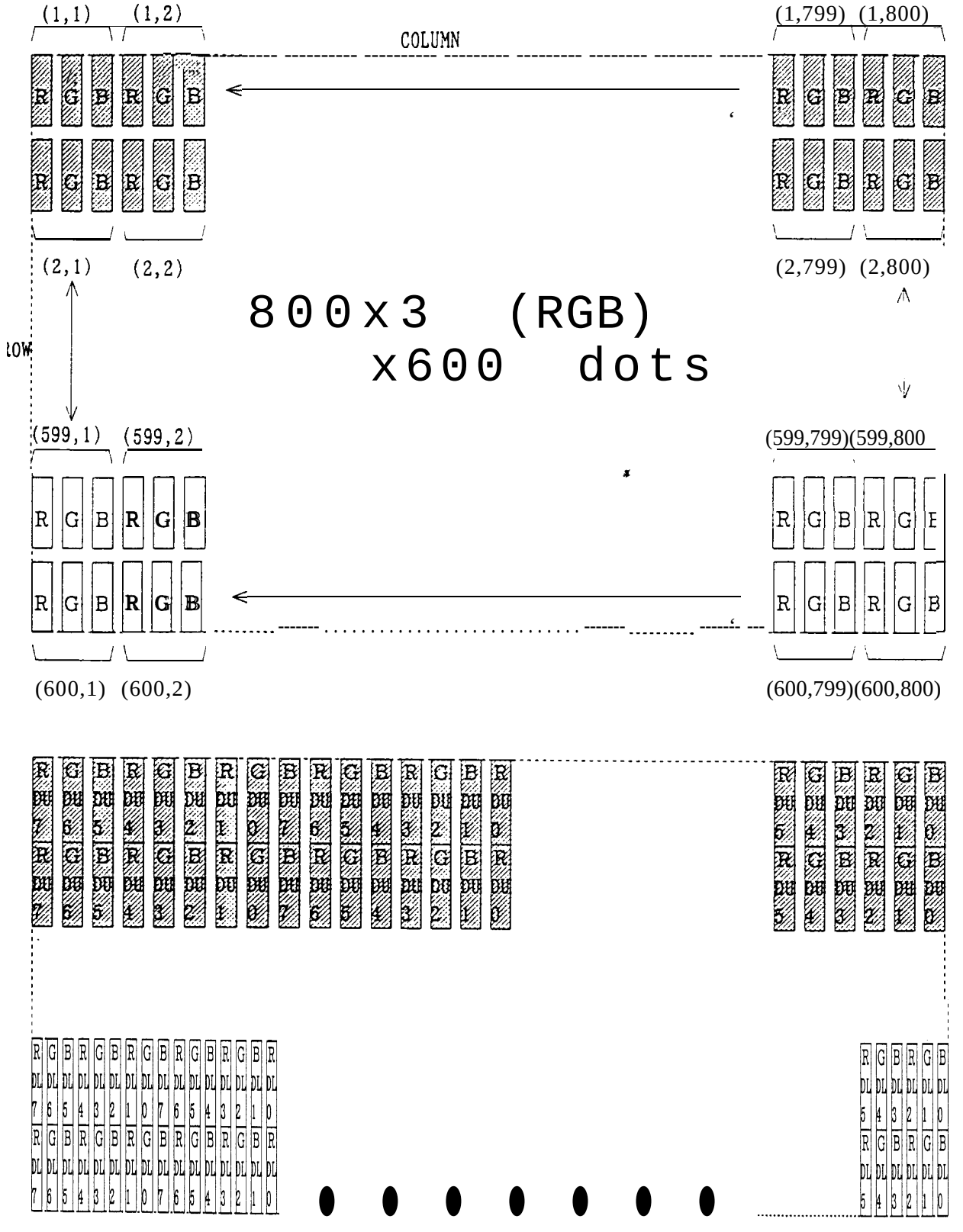


Fig.1 Dot chart of display area

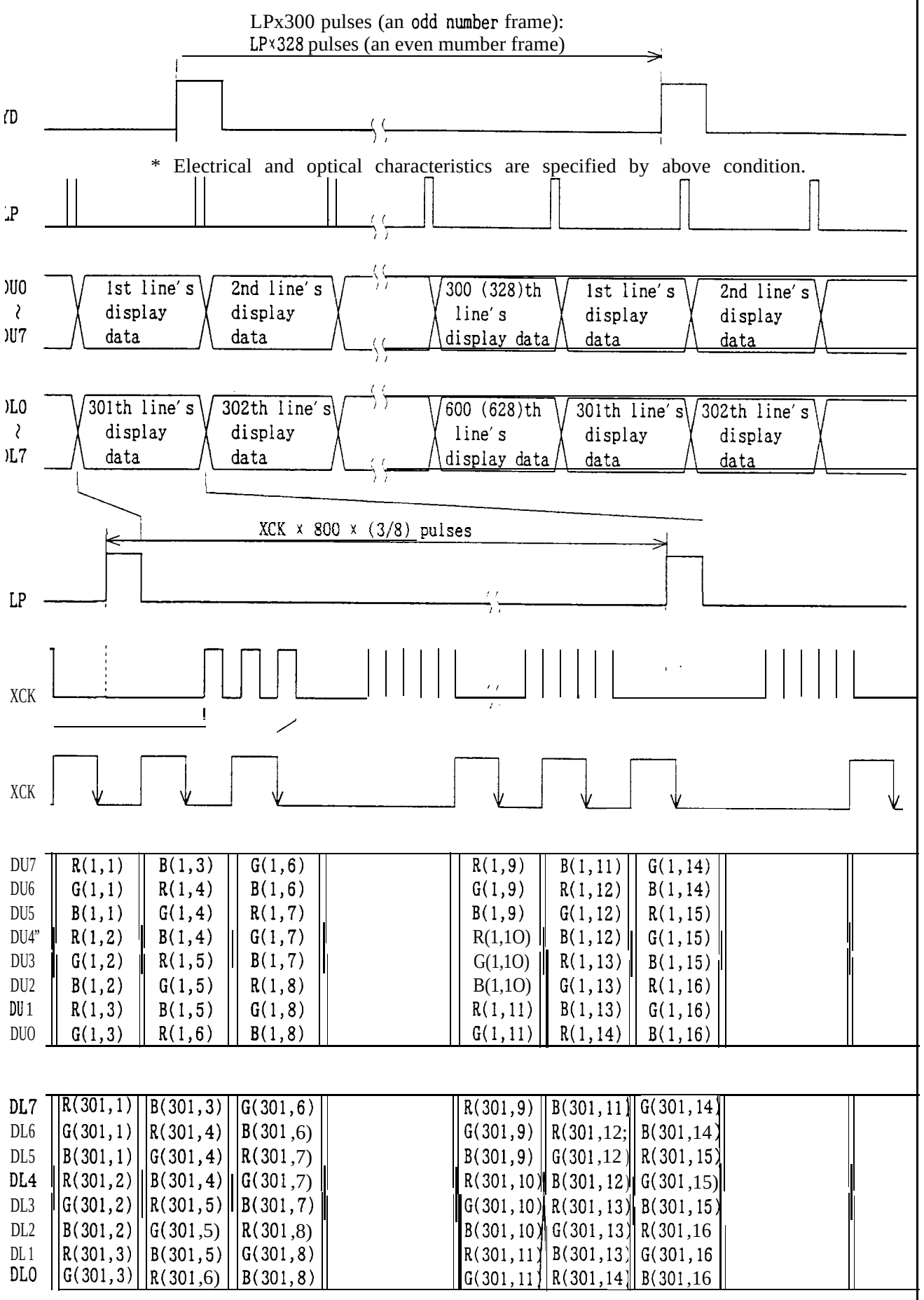


Fig.2 Data input timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle *1	tFRM	8.3		16.4	ms
YD signal "H" level set up time	tHYS	100			ns
"H" level hold time	tHYH	100			ns
"L" level set up time	tLYS	100			ns
'L" level hold time	tLYH	40			ns
LP signal "H" level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	50			ns
"H" level clock width	tWCKH	20			ns
"L" level clock width	tWCKL	20			ns
Data set up time	tDS	17			ns
hold time	tDH	23			ns
LP ↑ allowance time from XCK ↓	tLS	200			ns
XCK ↑ allowance time from LP ↓	tLH	200			ns
Input signal rise/fall time	tr,tf			*1 13	ns

*1 When LCD module is operated by high speed of XCK(Shift clock), (tWCK-tWCKH-tWCKL)/2 is maximum.

※ The intervals of one LP fall and the next must be always the same, and LPs must be input continuously.
The intervals must be 70 us Max.

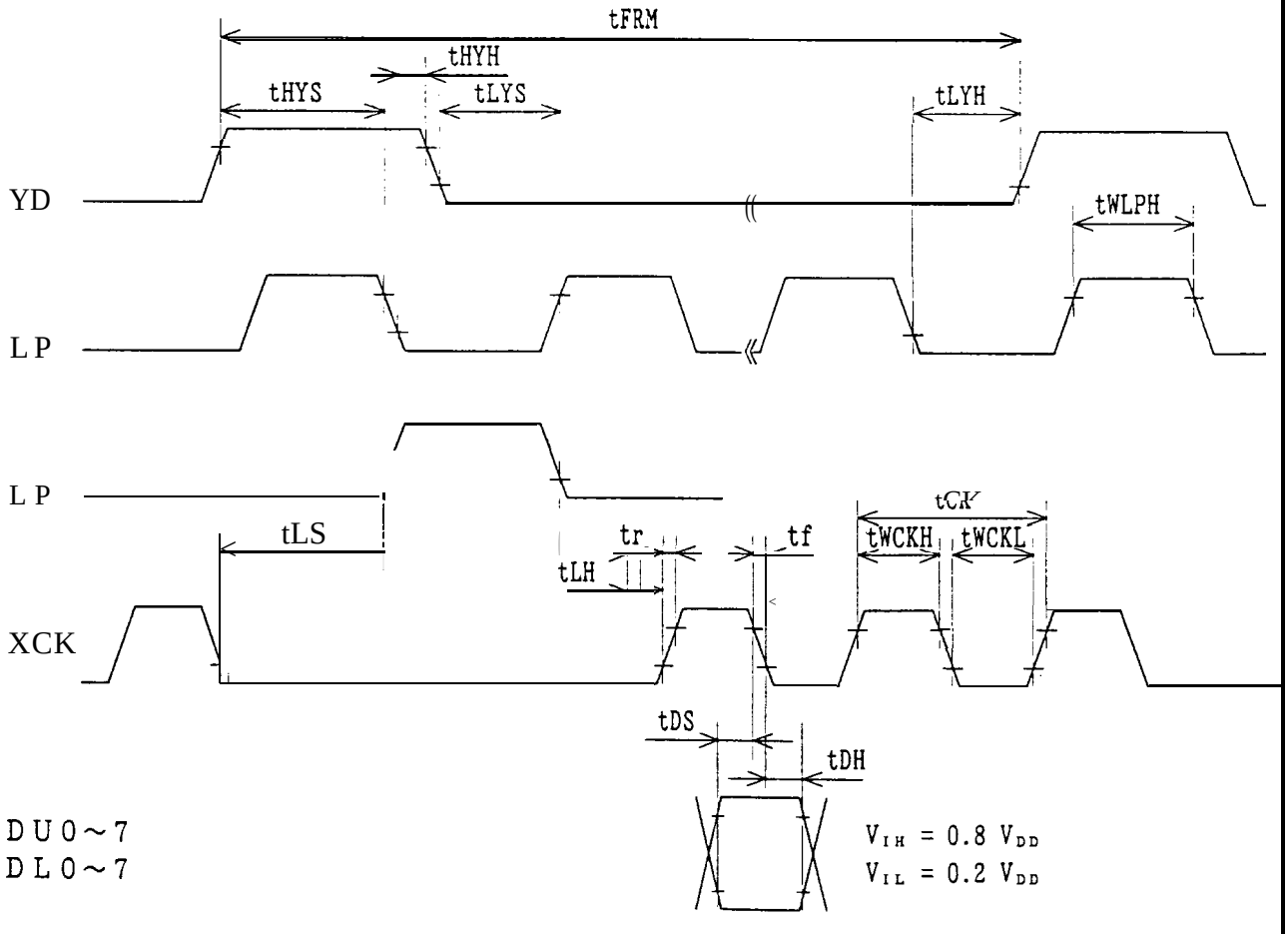


Fig.3 Interface timing chart

*2 LCD unit functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of 120 Hz).
Owing to the characteristics of LCD Unit,''shadowing" will become more eminent as frame frequency goes up, while flicker will be reduced.

According to our experiments,frame cycle of 8.33 ms Min. or frame frequency of 120 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgement of display quality is subjective and display quality such as "shadowing" is pattern dependent,it is recommended that decision of frame frequency, to which power consumption of the LCD unit is propotional,be made based on your own through testing on the LCD unit with every possible patterns displayed on it.

6. module Driving Method

6.1 Circuit configuration

Fig.9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 800x3 (R,G,B)x600 dots as shown in Fig.1.
The interface is single panel with double drive to be driven at 1/300(328 duty ratio (1/300:an odd number frame, 1/328:an even number frame)

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (800x3 R,G,B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal(XCK).

When input of one row (800 x 3,R,G,B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 800 x 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 640x3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 300(328)th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Contro Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the disp ay module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DUO-7 and DL0～7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI′s.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requ res the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown n Fig. 3 and Table 7.

7.Optical Characteristics

Ta=25 ℃, V_{DD} = 3.3 V, Vcon-V_{ss} = Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0°$) will be MAX.

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>5.0 ey=o "	-30	-	30	dgr.	Notel)
		θy	θx=0°	-15	-	20	dgr.	
Contrast ratio		co	θx=θy=0°	15	25	-	-	Note2)
Response time	Rise	τr	θx=θy=0°	-	220	330	ms	Note3)
	Decay	τd	θx=θy=0°	-	80	120	ms	
module chromaticity	White	x	θx=θy=0°	·	0.290	-	-	
		Y	θx=θy=0°	-	0.340	-	-	

Note 1) The viewing angle range is defined as shown Fig.4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixels "White" at Vmax}}{\text{Luminance(brightness) all pixels "dark " at Vmax}}$$

Vmax is defined in Fig.6.

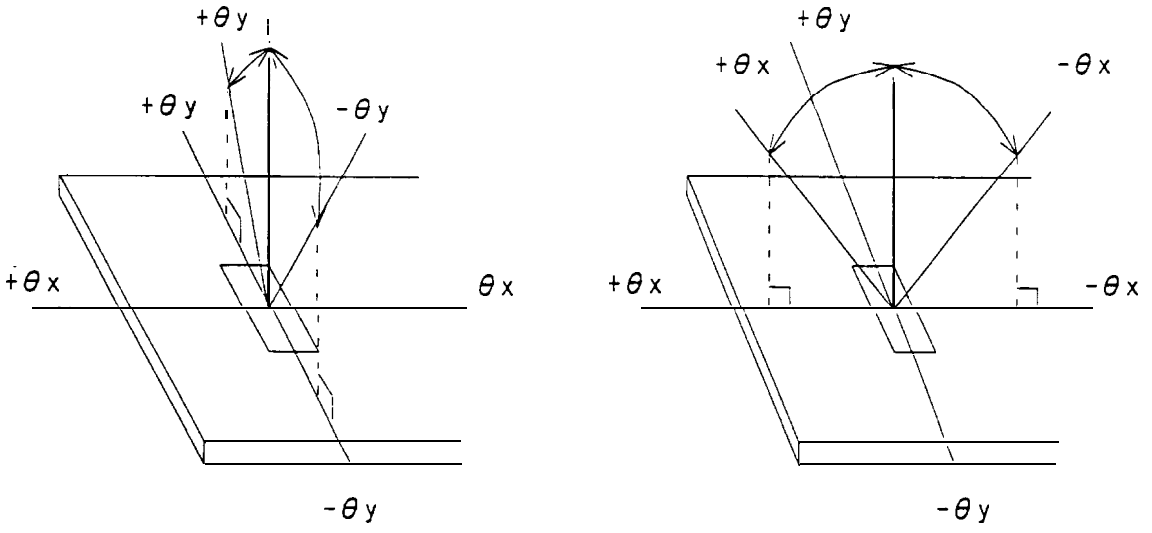
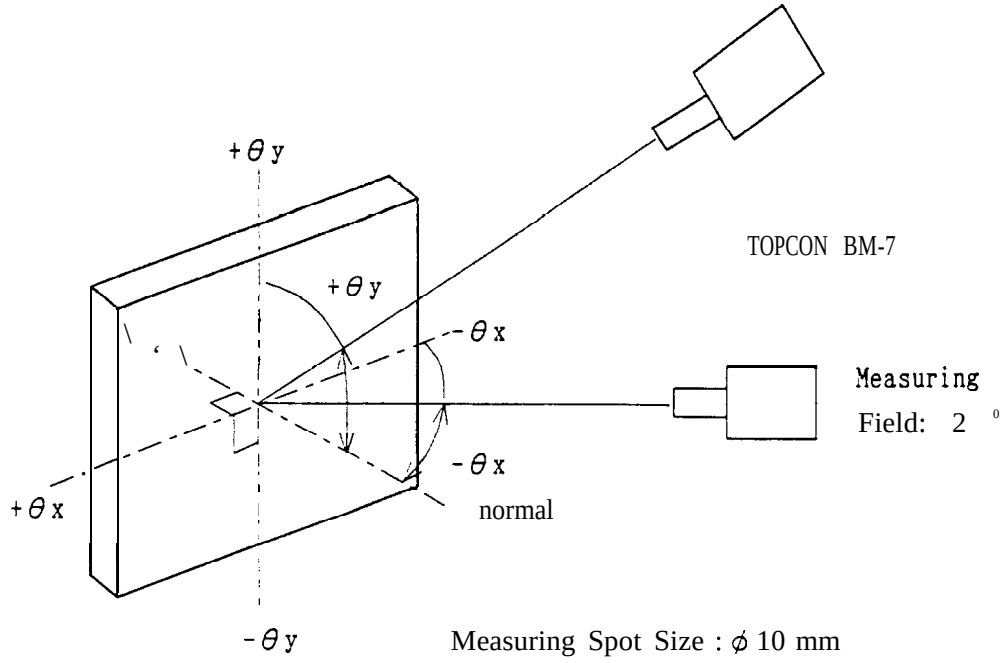


Fig.4 Definition of Viewing Angle

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig.8.



Measuring Spot Size : ϕ 10 mm

θx : Angle from "normal"to viewing surface rotated about the horizontal axis.

θy : Angle from "normal"to viewing surface rotated about the vertical axis.

Fig.5 Optical Characteristics Test Nethod I

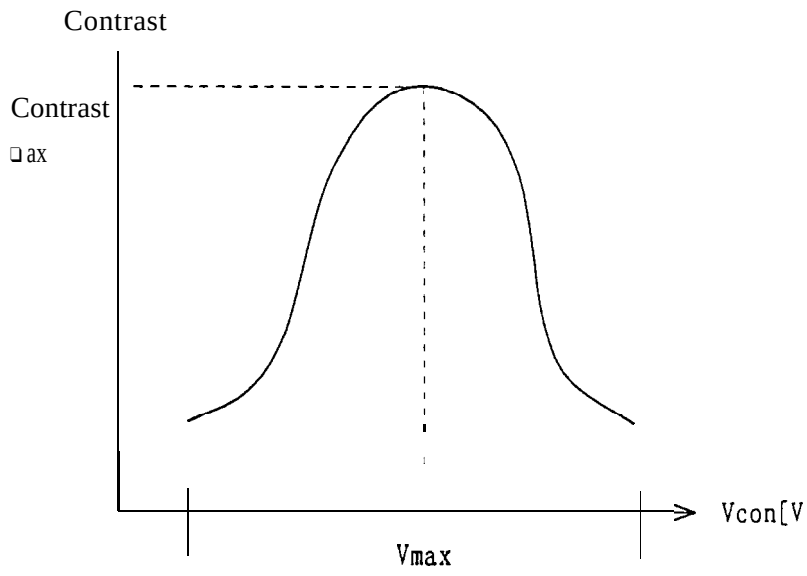
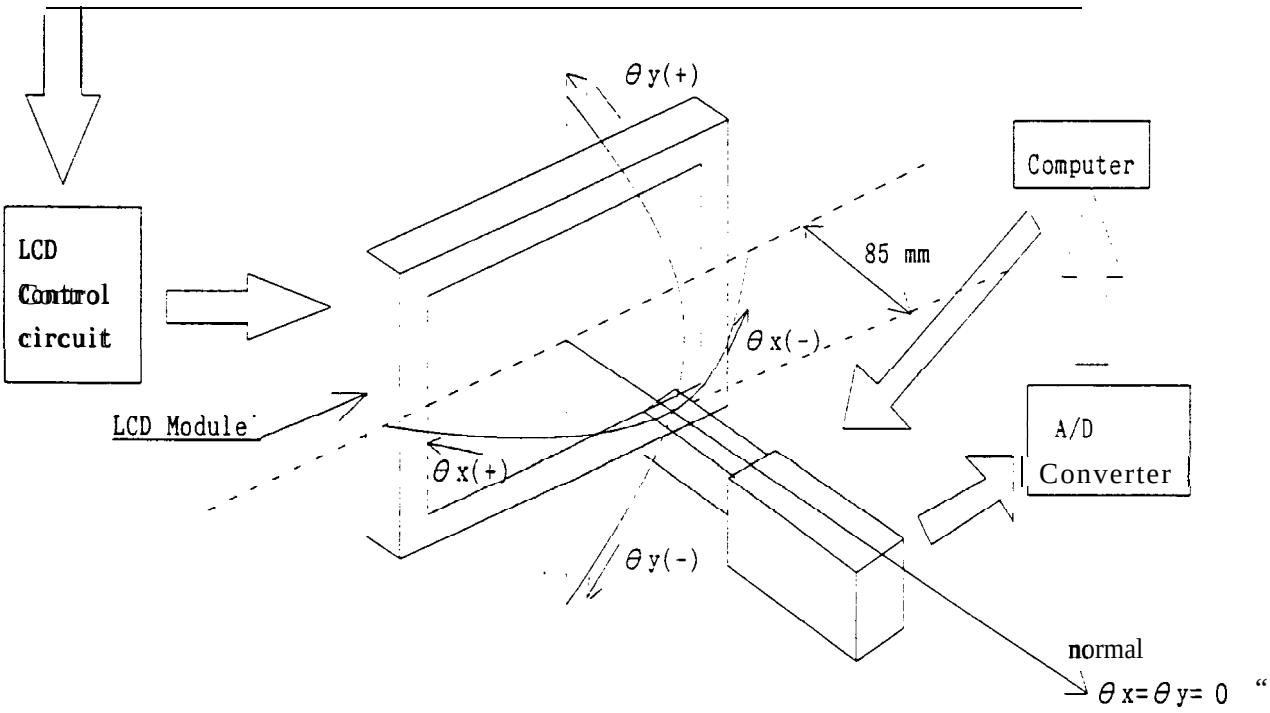


Fig.6 Definition of Vmax

(Response Measurement)

Ta=25 "C

In dark room



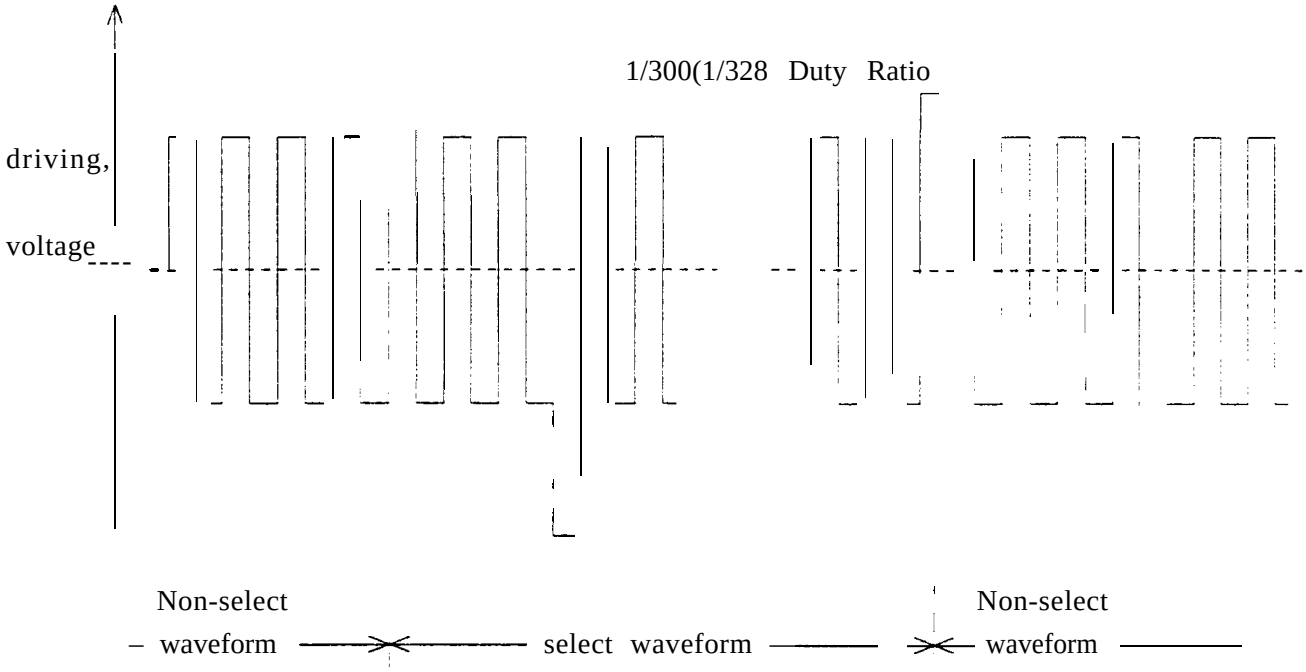
TOPCON BM7 + quartz fiber

(Measurirg Spot Size: ϕ 10 mm ,

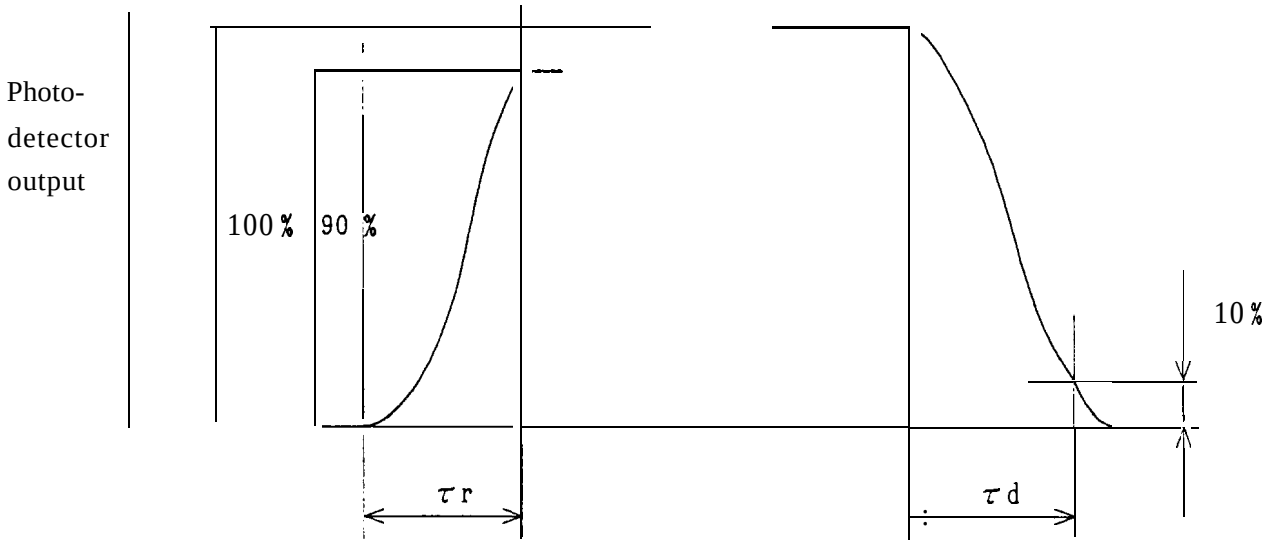
Measuring Field: 2 ")

Fig.7 Optical Characteristics Test Method II

[Drive waveform]



[Response waveform]



τr: Rise time

τd: Decay time

Fig.8 Definition of Response Time

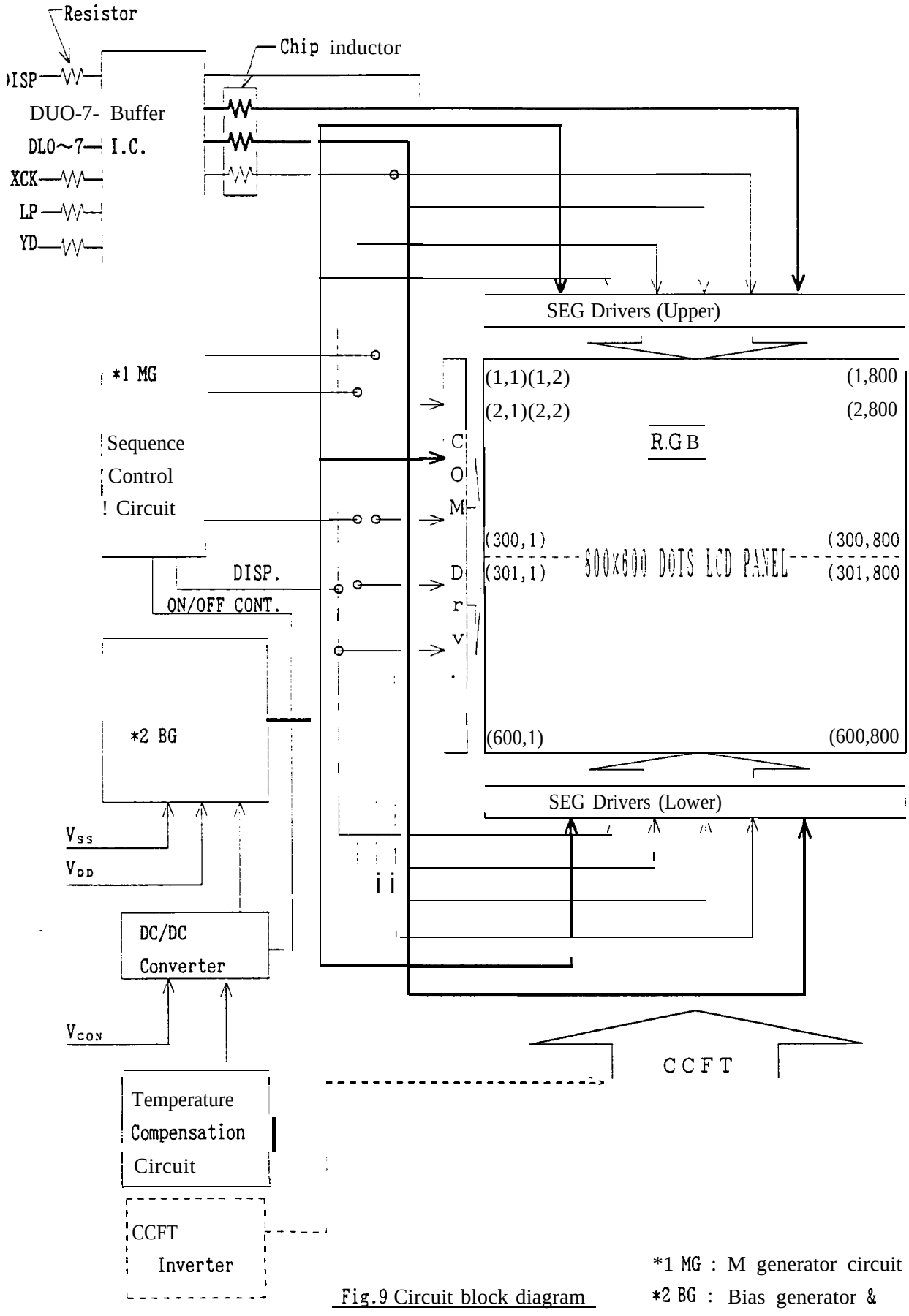
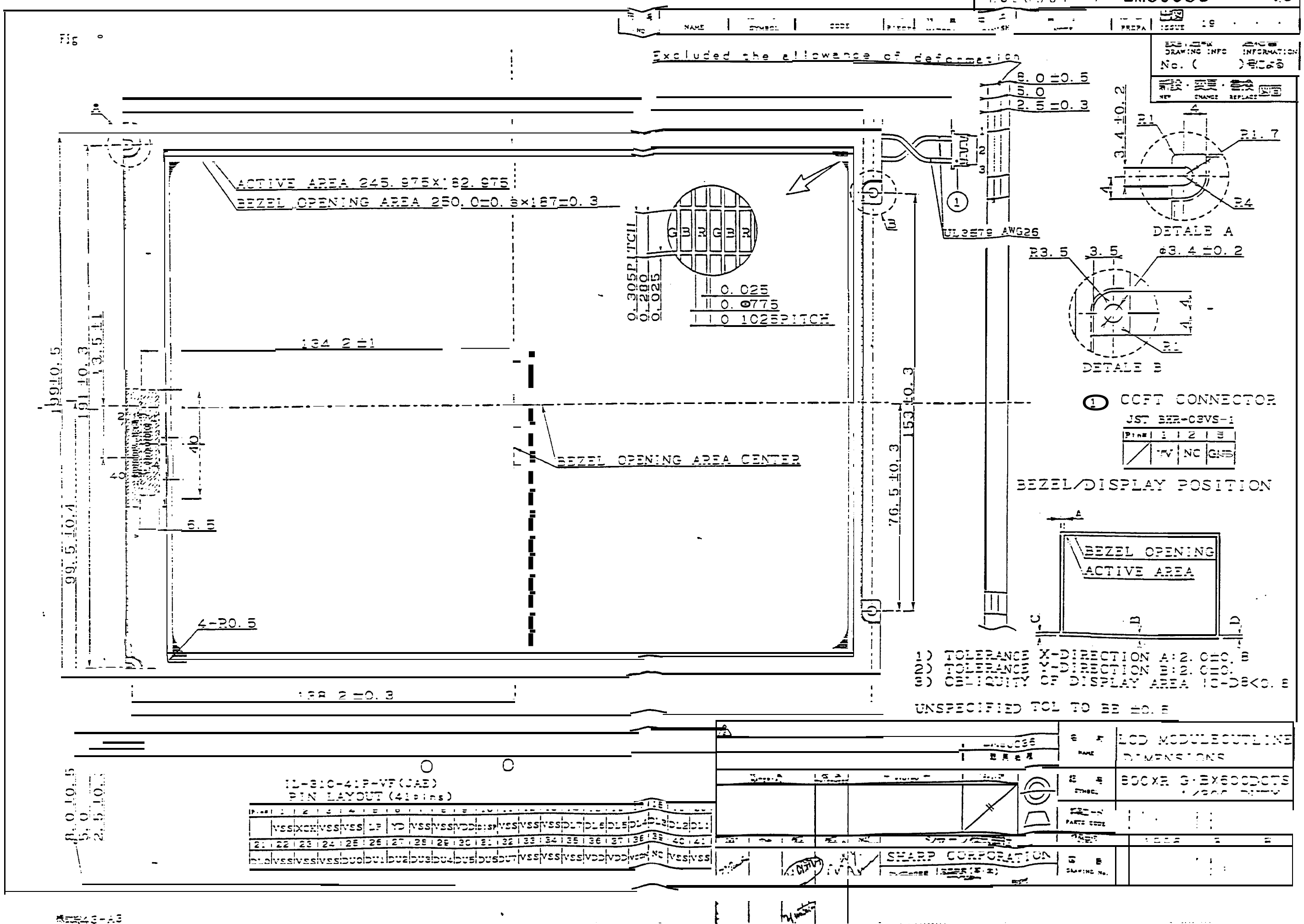


Fig.9 Circuit block diagram

*1 MG : M generator circuit

*2 BG : Bias generator & Protection circuit

Fig 6


Excluded the allowance of deformation
8.0±0.5
5.0
2.5±0.3
ACTIVE AREA 245.975×182.975
BEZEL OPENING AREA 250.0±0.8×187±0.3
0.305PITCH
0.280
0.025
0.025
0.775
0.1025PITCH
134.2±1
191±0.3
99.5±0.4
40
40
6.5
4-R0.5
BEZEL OPENING AREA CENTER
153±0.3
70.5±0.3
UL3575 AWG26
R1
R1.7
3.4±0.2
4
R4
DETALE A
R3.5
3.5
φ3.4±0.2
4.4
R1
DETALE B
① CCFT CONNECTOR
JST BHR-03VS-1
Pins | 1 | 2 | 3
HV | NC | GND
BEZEL/DISPLAY POSITION
BEZEL OPENING
ACTIVE AREA
1) TOLERANCE X-DIRECTION A:2.0±0.8
2) TOLERANCE Y-DIRECTION B:2.0±0.
3) OBLIQUITY OF DISPLAY AREA |C-D|<0.8
UNSPECIFIED TOL TO BE ±0.5
8.0±0.5
5.0
2.5±0.3
IL-81C-41P-VF(JAE)
PIN LAYOUT (41pins)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Vss XCK Vss Vss LP YD Vss Vss Vcc R,G,B Vss Vss Vss DL DL DL DL DL DL DL
21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41
DL Vss Vss Vss Vss DU DU DU DU DU DU DU Vss Vss Vss Vcc Vcc Vcc NC Vss Vss
LCD MODULE OUTLINE DIMENSIONS
SHARP CORPORATION